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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,891	04/15/2004	Marc E. Goldfarb	A5WI2646US	8986

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,891	GOLDFARB ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10-14,16-18,22-26,29 and 30* is/are rejected.

7)☒ Claim(s) *3,9,15,19-21,27-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/05/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-30 are presented in the instant application according to the Applicants' amendment filed on 01/17/2006.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 22-24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22 recites the limitation "said pulse trains" in lines 9-10. There is insufficient antecedent basis for this limitation in the claim.

Claims 23-24 are also rejected under 35 U.S.C. 112, second paragraph because of their dependencies on independent claim 22.

Clarification/Correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a

U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-2, 5-7, 11 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Cho (U.S. Patent No. 6,917,229).

With respect to claims 1 and 11, Cho discloses, in Figure 1, a reference signal generator, comprising an oscillator *(inherent since clock signal Clock is generated by an oscillator)* that provides an oscillator signal [Clock]; a buffer amplifier [140] having an adjustable amplifier gain that corresponds to a gain control signal [output from 130] and coupled to process the oscillator signal into a reference signal [output form 140] that has a reference amplitude; and a controller [120,130] that adjusts the amplifier gain/gain control signal in response to the reference amplitude.

With respect to claim 2, Cho discloses, in Figure 1, that the amplifier gain corresponds to a gain control signal [output from 130] and the controller includes at least one comparator [120] that responds to the reference signal and provides a pulse train [output from 120] when the reference amplitude exceeds a predetermined threshold signal *(in this case the threshold signal would be the clock signal)*; in response to the pulse train, a counter [130] that provides the gain control signal to thereby reduce the amplifier gain until the reference amplitude no longer exceeds the threshold signal *(when there is no error between the two signals Fbclk and Clock)*.

With respect to claim 5, Cho discloses, in Figure 1, that the buffer amplifier [140] includes at least one set of current generators *(delay elements/ inverters which form the delay line/amplifier 140)* that provide a current with a current amplitude that corresponds to the gain control signal [from 130] and an inverter *(inherently as one of the delay elements of the delay*

line/amplifier) that carries the current to provide the reference signal with the reference amplitude thereby corresponding to the gain control signal.

With respect to claim 6, Cho discloses, in Figure 1, that the current generators *(delay elements/ inverters which form the delay line/amplifier 140)* are configured with binarily-related currents so that the current amplitude has a binary relationship to the gain control signal *(from counter and decoder130)*.

With respect to claim 7, Cho discloses, in Figure 1, that the controller includes a counter [130] set to an initial count that maximizes an amplifier gain and coupled to provide a subsequent count of a clock signal that reduces the amplifier gain; and a comparator that terminates the subsequent count in response to a reference amplitude and a predetermined threshold amplitude.

With respect to claim 18, Cho discloses, in Figure 1, that the controller includes a clock that provides a clock signal; a counter [130] that counts the clock signal to thereby generate digital gain control signal [output from 130]; and a comparator [120] that passes the clock signal to the counter in response to a comparison of said reference signal and a threshold signal.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Donnelly et al. (U.S. Pat. No. 6,642,746).

With respect to claims 4 and 17, Cho discloses all of the claimed limitations as expressly recited in claims 1-2, 11 and 18 except for the comparator comprising a differential pair of transistors.

Donnelly et al. discloses in Fig. 3, a phase comparator comprising a differential pair of transistors [49, 50] that determines the gain control signal in response to the reference signal [Vref] and the threshold signal [Vin2].

To configure the circuit of Cho with a comparator including comprising a differential pair of transistors that determines the gain control signal in response to the reference signal and the threshold signal as taught by Donnelly et al. for minimized phase detector error would have been obvious to one of ordinary skill in the art at the time of the invention since Donnelly et al. teaches that such configuration would accurately detects the phase/gain difference between the two inputs having different voltage swing characteristics *(see Donnelly et al., col. 1, lines 32-34).*

7. Claims 8, 12-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Ooishi (U.S. Pat. No. 6,404,258).

With respect to claims 8, 12-14 and 16, Cho discloses all of the claimed limitations as expressly recited in claims 1 and 11, except for the buffer amplifier including a plurality of current generators and each of the plurality of the current generators includes a plurality of resistors; and a plurality of switches that selectively access resistors in response to the gain

control signal to thereby adjust amplifier gain and an output switch that couples selected resistors to the reference port in response to the oscillator signal.

Ooshi discloses in Fig. 34, a buffer amplifier including a plurality of current generators [82a-f, 83a-f] and each having a plurality of resistors *(82d-f, since transistors being equivalent to resistors as shown in fig. 7B of Morimura et al. (U.S. Patent No. 6,556,935)*; and a plurality of switches [82a-b] that selectively access the resistors and an output switch [80b-c] that couples selected resistors to the reference port.

To configure the circuit of Cho with a buffer amplifier including a plurality of current generators with a plurality of resistors and a plurality of switches that selectively access the resistors as taught by Ooishi so that the delay can be set to a desired value would have been obvious to one of ordinary skill in the art at the time of the invention since Ooishi teaches that such configuration would facilitate a delay circuit that operates with stability irrespective of the operating environment can be implemented *(see Ooishi., col. 32, lines 29-40)*.

8. Claims 10 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Lin et al. (U.S. Pub. No. 2005/0093638 A1).

With respect to claims 10 and 25, Cho discloses all of the claimed limitations as expressly recited in claim 1, except for the oscillator which generated the reference clock signal specifically being a digitally-controlled crystal oscillator.

Lin et al. discloses, in Fig. 2 and paragraph [0007], a digitally-controlled crystal oscillator and its advantages.

To configure the circuit of Cho with a digitally-controlled crystal oscillator as taught by Lin et al. to control more precisely the resonant frequency of the crystal oscillator by including a processing portion that monitors the resonant frequency produced by a crystal oscillator and alters the resonant frequency of the crystal oscillator by changing the capacitive loading on the crystal oscillator to tune the frequency of the crystal oscillator would have been obvious to one of ordinary skill in the art at the time of the invention since such circuit arrangement of the digitally-controlled crystal oscillator for the stated purpose has been a well known practice as evidenced by the teachings of Lin et al. *(see Lin et al., paragraph [0007], lines 4-13).*

9. Claims 26 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Fiscus (U.S. Patent No. 6,492,852) and in view of Li (U.S. Pub. No. 2005/0046495).

With respect to claim 26, Cho discloses a synthesizer comprising a buffer amplifier [110] having an adjustable amplifier gain and coupled to process a reference oscillator signal [Clock, generated from an oscillator] into a reference signal that has a reference amplitude; and a controller [120, 130] that adjusts the amplifier gain in response to the reference amplitude.

Cho fails to disclose a first frequency divider, a second frequency divider, a voltage-controlled oscillator and a phase detector that provides a control signal to the voltage-controlled oscillator;

Fiscus discloses, in Fig. 5, a locked loop comprising a first frequency divider [116]; a second frequency divider.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure a divider circuit to divide the input clock signal of Cho locked loop circuit as taught by Fiscus in order to provide the required reduced frequency of the clock signal that propagates through the delay line circuit hence reduce power consumption since such circuit arrangement of the divider circuit for the stated purpose has been a well known practice as evidenced by the teachings of Fiscus *(see Fiscus, col. 4, lines 5-9)*.

The combined teaching of Cho and Fiscus fails to disclose fails to disclose a voltage-controlled oscillator and a phase detector that provides a control signal to the voltage-controlled oscillator.

Li discloses, in Figs. 6-7, a circuit encompassing two locked loop circuits [Fig. 6] and the details of one of the locked loop circuits [Fig.7] with a voltage-controlled oscillator [300] and a phase detector [700] that provides a control signal to the voltage-controlled oscillator.

To configure the circuit of the combined teaching of Cho and Fiscus in the same arrangement as shown in Fig. 6 and with a voltage-controlled oscillator and a phase detector [Fig. 7] as taught by Li for phase noise cleaning up would have been obvious to one of ordinary skill in the art at the time of the invention since Li teaches that such configuration would minimize the phase noise thus improve the circuit performance *(see Li, paragraph [0034] col. 1, lines 32-34)*.

With respect to claim 29, the combined teaching of Cho, Fiscus and Li discloses that the controller [120, 130] includes a counter set to an initial count that maximizes the amplifier gain and coupled to provide a subsequent count of the clock signal that reduces the amplifier gain;

and a comparator that terminates the subsequent count to when the reference amplitude reaches a threshold amplitude.

12. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Fiscus (U.S. Patent No. 6,492,852) and in view of Li (U.S. Pub. No. 2005/046495), as applied in claim 26, and further in view of Ooishi (U.S. Pat. No. 6,404,258).

With respect to claim 30, the combined teaching of Cho, Fiscus and Li discloses all of the claimed limitations as expressly recited in claim 26, except for the buffer amplifier including a plurality of resistors; and a plurality of switches that selectively access the resistors in response to the controller to thereby adjust amplifier gain.

Ooshi discloses in Fig. 34, a buffer amplifier including a plurality of current generators [82a-f, 83a-f] and each having a plurality of resistors *(82d-f, since transistors being equivalent to resistors as shown in fig. 7B of Morimura et al. (U.S. Patent No. 6,556,935)*; and a plurality of switches [82a-b] that selectively access the resistors and an output switch [80b-c] that couples selected resistors to the reference port.

To configure the circuit of the combined teaching of Cho, Fiscus and Li with a buffer amplifier including a plurality of current generators with a plurality of resistors and a plurality of switches that selectively access the resistors as taught by Ooishi so that the delay can be set to a desired value would have been obvious to one of ordinary skill in the art at the time of the invention since Ooishi teaches that such configuration would facilitate a delay circuit that operates with stability irrespective of the operating environment can be implemented *(see Ooishi., col. 32, lines 29-40)*.

Allowable Subject Matter

10. The Applicant is noted that claim 22 must be corrected to overcome 112 2nd paragraph rejection set forth in this office action.

11. Claims 3, 9, 15, 19-24 and 27-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A generator, in which the controller further includes a generator that responds to a first clock signal to provide a second clock signal, an enable signal and a subsequent disable signal; a first gate that passes the second clock signal in response to the enable signal and blocks the second clock signal in response to the disable signal; and a second gate that passes the second clock signal from the first gate to the counter in response to the pulse train, as called for in claim 3;

b) A generator, in which the comparator comprises upper and lower comparators that respectively respond to upper and lower predetermined threshold signals, as called for in claim 9;

c) A generator, in which the controller further includes a differential pair of amplifiers that transfers a common mode level of the reference signal to the string of resistors, as called for in claim 15;

d) A generator, in which the controller further includes a gate inserted to pass the clock signal to the counter in response to the comparator, as called for in claim 19;

e) A generator, in which the controller includes upper and lower comparators that generate pulse trains when the reference signal exceeds predetermined threshold signal; and a gate that passes the clock signal to the counter in response to the pulse trains, as called for in claim 22;

f) A synthesizer, in which the controller further includes a gate coupled to pass the clock signal to the counter; and a generator that provides an enable signal to enable the gate and a subsequent disable signal to disable the gate, as called for in claim 27; and

g) A synthesizer, in which the controller further includes a differential pair of transistors that provide a common mode level of the reference signal; and a resistor string that provides the threshold amplitude in response to the common mode level, as called for in claim 28.

Remarks

13. Applicant's arguments filed 01/17/2006 have been fully considered but they are not persuasive.

With respect to Applicants' argument, on page 12, second paragraph, regarding claim 1, lines 4-5, Applicants state that Cho fails to teach an amplifier that processes an oscillator signal into a reference signal with an amplifier gain that is adjusted by a controller. The Examiner respectfully disagrees. Although Cho is not seen to expressly disclose "an amplifier" in the disclosure, instead Cho discloses a delay line [140]; however; a) first, as stated in MPEP § 2163.02, the subject matter of the claimed need not be described literally (i.e. using the same terms or *in haec verba)* in order for the disclosure to satisfy the description requirement; and, b) second, the term should be given its broadest reasonable interpretation and take on the ordinary and customary meaning attribute to it by those of ordinary skill in the art, unless the term is

defined in the specification; thus, the broadest reasonable interpretation of the term "amplifier" would be a circuit having a voltage gain, which is a quotient resulting from the output voltage divided by the input voltage and the delay line 140 carries a voltage gain which is a quotient resulting from output voltage of 140 divided by input voltage of 140. Cho's Fig. 1 discloses an amplifier that processes an oscillator signal [Clock] into a reference signal with an amplifier gain [gain from 140] that is adjusted by a controller [120, 130]. Hence, Cho indeed discloses the claimed limitations.

Similar argument has been addressed by the Applicants on page 12, fifth paragraph, regarding claim 11 and again on page 13, regarding claim 26; it is suggested to refer to the above paragraph for response(s).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

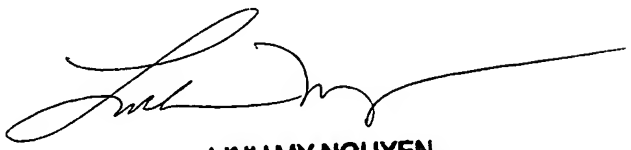
Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN



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PRIMARY EXAMINER